Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S2	1018	(257/E25.023).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/28 12:31
S5	121	(257/505).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/28 12:32
S4	784	(257/510).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/28 12:32
S3	87	(257/E27.009).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/28 12:32
S9	235	(257/396).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/28 12:33
S8	137	(257/395).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/28 12:33
S7	424	(257/528).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/28 12:33
S6	302	(257/520).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/28 12:33
S10	204	(257/397).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/28 12:34
S1	72	(257/E25.01).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/04/29 08:59
S12	90260	semiconductor and ((trench$3 or groov$3 or recess$4) same (isolat$4 or insulat$4 or dielectric or oxide))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/29 09:06
S13	76746	semiconductor and ((trench$3 or groov$3 or recess$4) with (isolat$4 or insulat$4 or dielectric or oxide))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/29 09:09

S15	1240	semiconductor and (((trench$3 or groov$3 or recess$4) with (isolat$4 or insulat$4 or dielectric or oxide)) same (polysilicon with (edge or periphery or peripheral or surround$3)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/29 09:11
S14	13225	semiconductor and (((trench$3 or groov$3 or recess$4) with (isolat$4 or insulat$4 or dielectric or oxide)) same polysilicon)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/29 09:12
S16	5530	semiconductor and (((trench$3 or groov$3 or recess$4) with (isolat$4 or insulat$4 or dielectric or oxide)) same polysilicon) and (thermal$3 with oxide)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/29 09:13
S17	4723	semiconductor and (((trench$3 or groov$3 or recess$4) with (isolat$4 or insulat$4 or dielectric or oxide)) same polysilicon) and (thermal$3 with oxide) and ((isolation or insulating or insulation or isolating or separation or separating) with (region or area or zone or portion))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/29 09:14
S19	972	semiconductor and (((trench$3 or groov$3 or recess$4) with (isolat$4 or insulat$4 or dielectric or oxide)) same polysilicon) and (thermal$3 with oxide) and (((isolation or insulating or insulation or isolating or separation or separating) with (region or area or zone or portion)) same (passive or resistor or capacitor or inductor)) not S15	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/29 09:16
S18	1122	semiconductor and (((trench$3 or groov$3 or recess$4) with (isolat$4 or insulat$4 or dielectric or oxide)) same polysilicon) and (thermal$3 with oxide) and (((isolation or insulating or insulation or isolating or separation or separating) with (region or area or zone or portion)) same (passive or resistor or capacitor or inductor))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/04/29 09:16